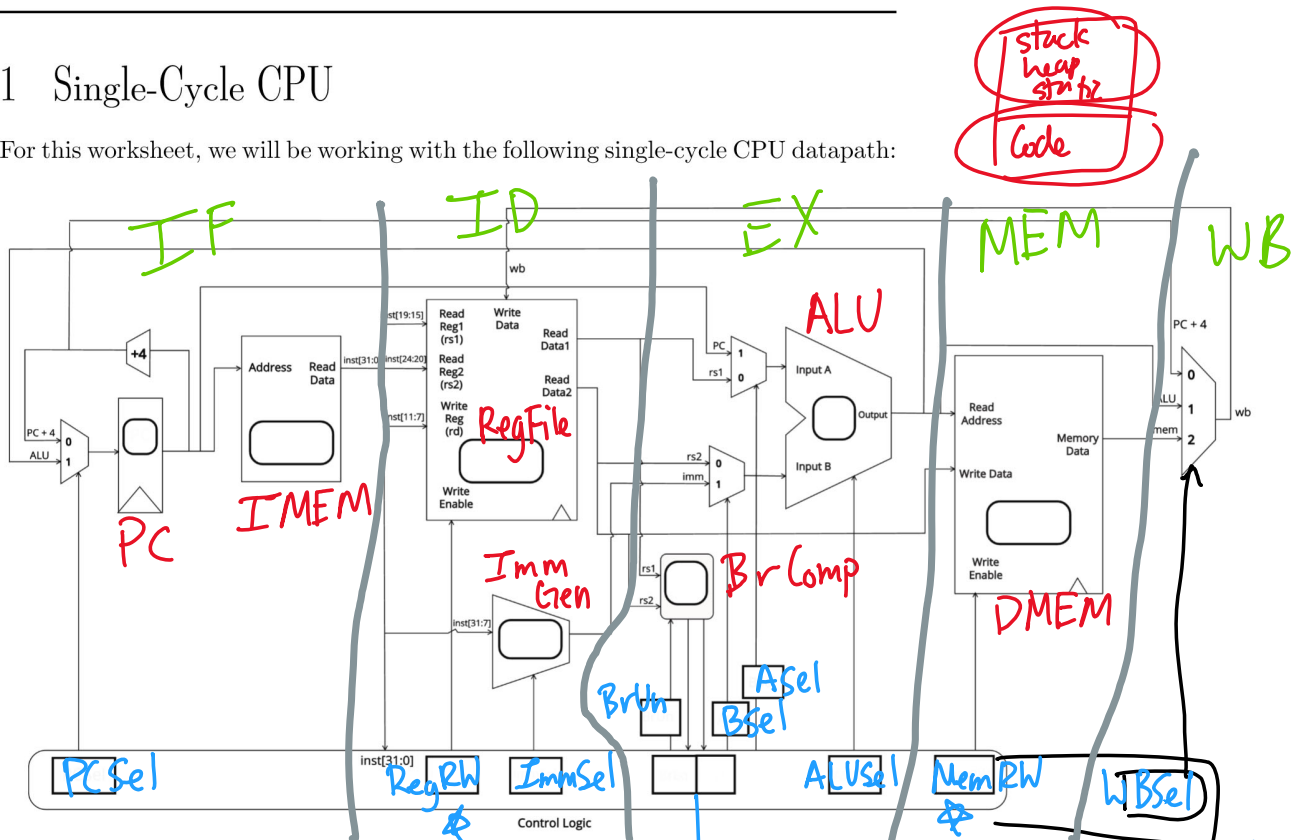


CS 61C  
Fall 2018

Single-Cycle Datapath  
Discussion 11: November 5, 2018

1 Single-Cycle CPU

1.1 For this worksheet, we will be working with the following single-cycle CPU datapath:



(a) On the datapath above, fill in each **round** box with the name of the datapath component, and each **square** box with the name of the control signal.

(b) Explain what happens in each datapath stage.

**IF** Instruction Fetch

get inst from mem

**ID** Instruction Decode

figure out what to do

**EX** Execute

perform ops + comparisons

**MEM** Memory

access mem

**WB** Writeback

store back to regs.

BrEq BrLt

Read: 0 ← default  
Write: 1

1.2 Fill out the following table with the control signals for each instruction based on the datapath on the previous page. Wherever possible, use \* to indicate that what this signal is does not matter.

*always matter*

	BrEq	BrLT	PCSel	ImmSel	BrUn	ASel	BSel	ALUSel	MemRW	RegWEn	WBSel
<u>add</u> ori	*	*	0	*	*	0	0	add	0	1	1
lw	*	*	0	S	*	0	1	add	1	0	*
<u>sw</u> beq	*	*	0	S	*	0	1	add	1	0	*
<u>jal</u> bltu	*	*	1	S	*	1	1	add	0	1	0

1.3 Clocking Methodology

- A **state element** is an element connected to the clock (denoted by a triangle at the bottom). The **input signal** to each state element must stabilize before each **rising edge**.
- The **critical path** is the longest delay path between state elements in the circuit. If we place registers in the critical path, we can shorten the period by **reducing the amount of logic between registers**.

For this exercise, assume the delay for each stage in the datapath is as follows:

IF: 200 ps    ID: 100 ps    EX: 200 ps    MEM: 200 ps    WB: 100 ps

(a) Mark the stages of the datapath that the following instructions use and calculate the total time needed to execute the instruction.

	IF	ID	EX	MEM	WB	Total Time
<u>add</u> ori	X	X	X		X	600 ps
lw	X	X	X	X	X	800 ps
<u>sw</u> beq	X	X	X	X		700
<u>jal</u> bltu	X	X	X		X	600

(b) Which instruction(s) exercise the critical path?

*lw*

(c) What is the fastest you could clock this single cycle datapath?

*1/800 ps = 1.25 GHz*

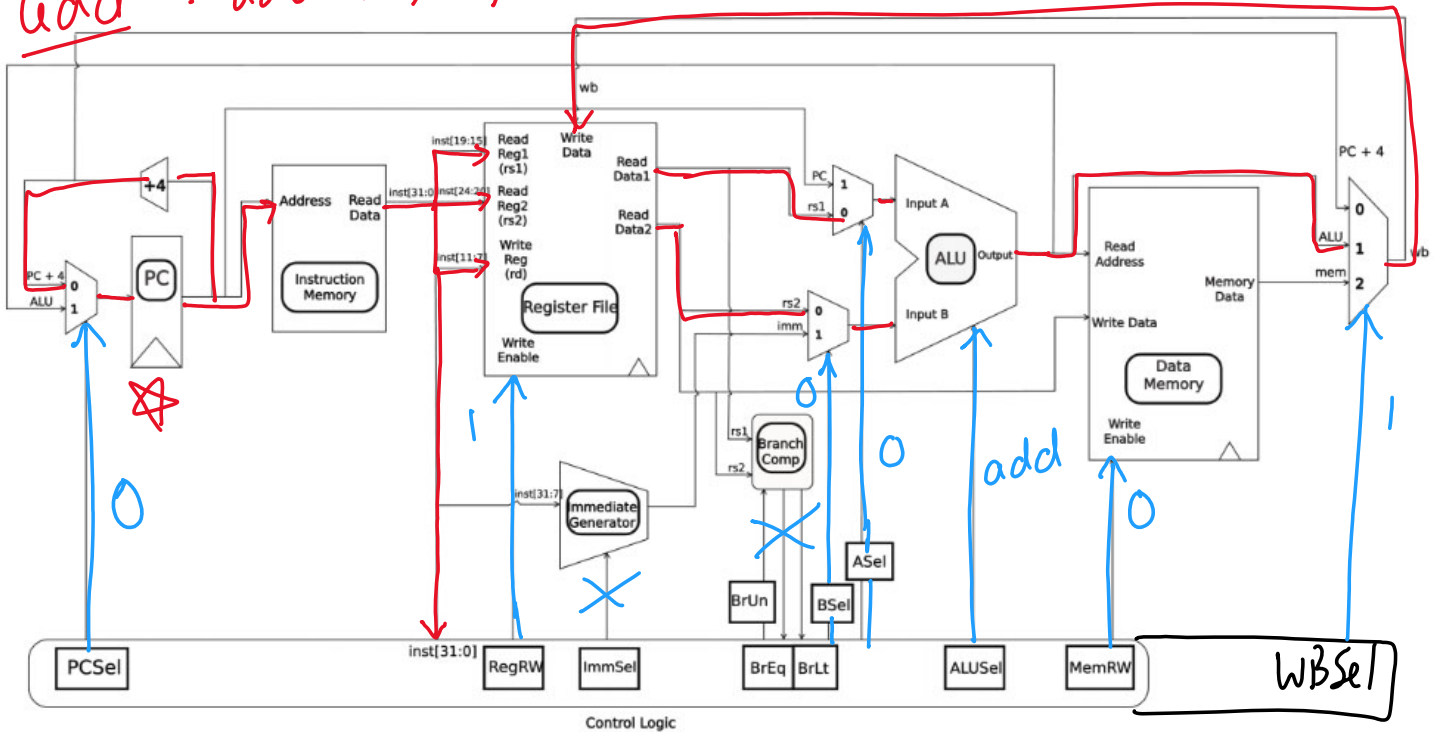
(d) Why is the single cycle datapath inefficient?

*idle component*

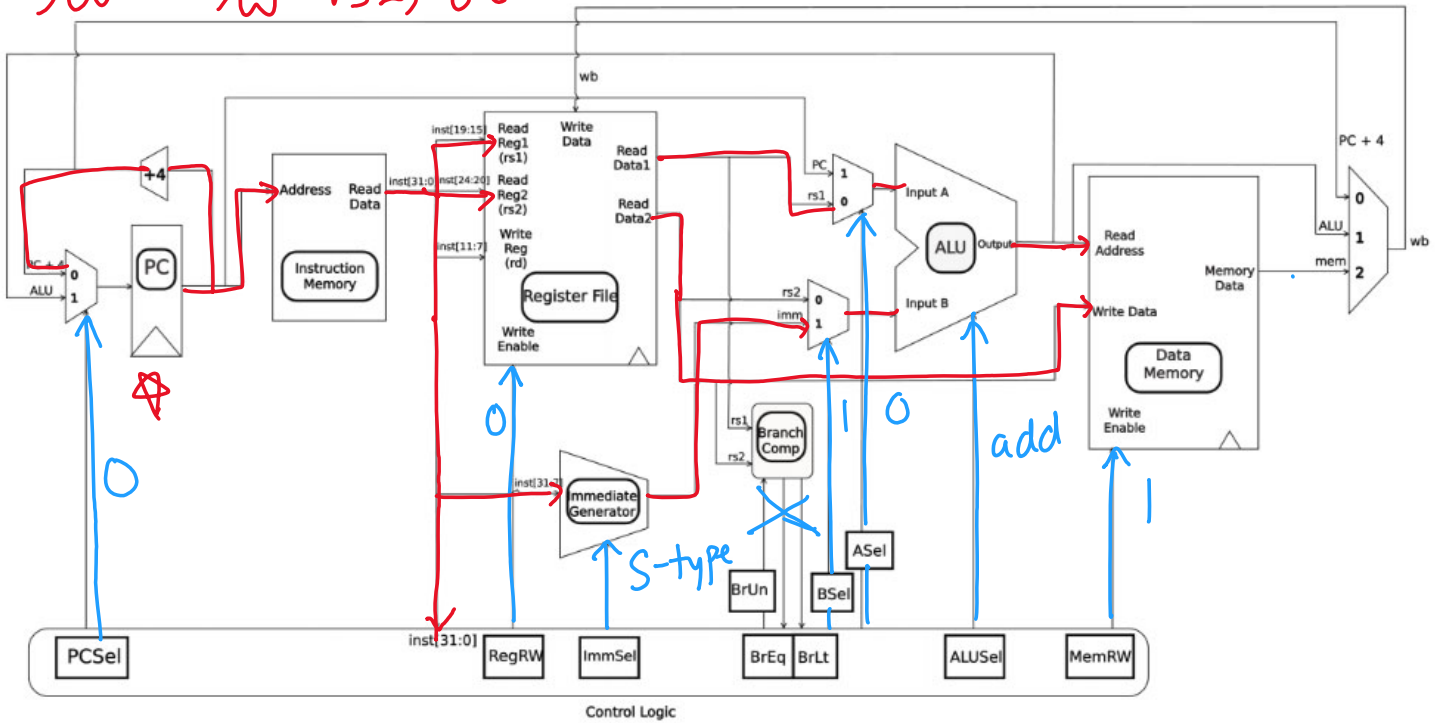
(e) How can you improve its performance? What is the purpose of pipelining?

*mult inst. at one time*

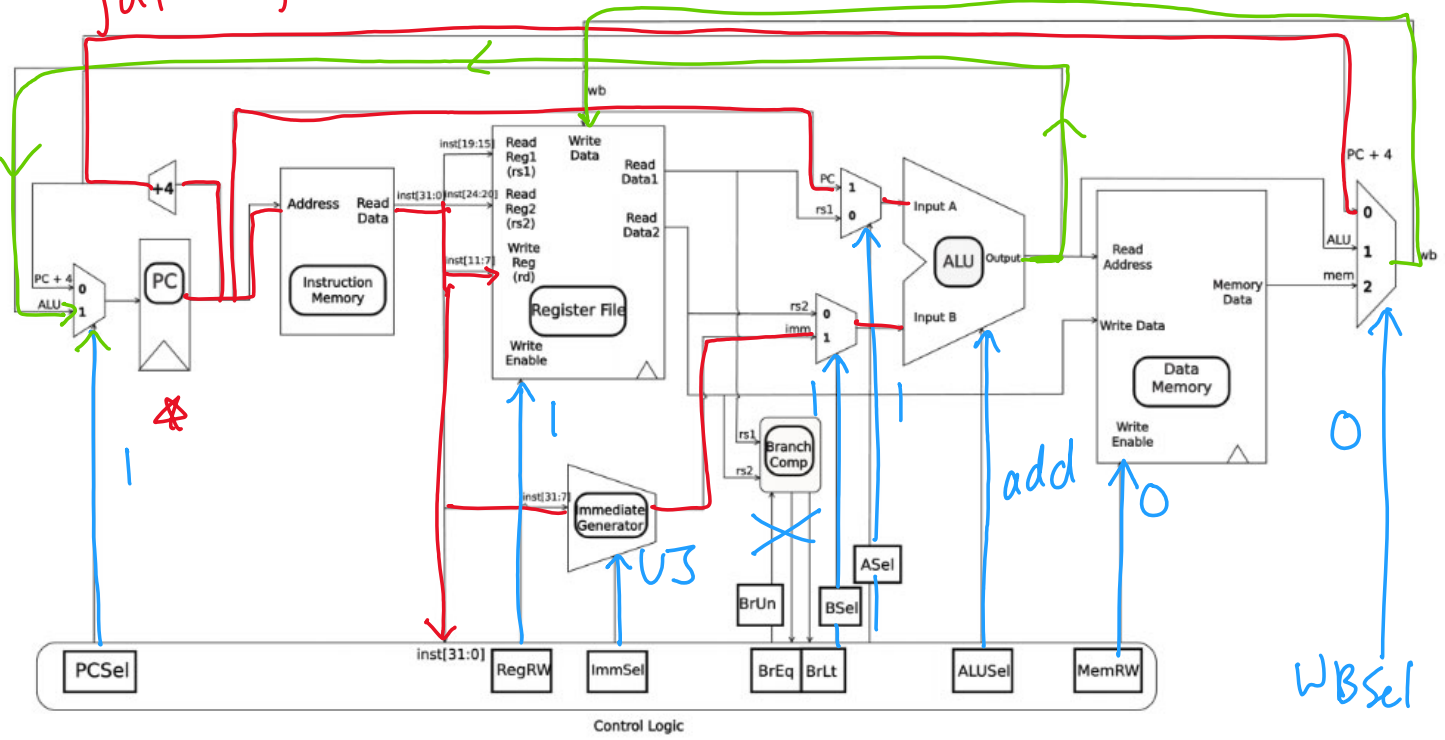
Add : add rd, rs1, rs2



SW sw rs2, 8(rs1)



jal jal ra, label



Control Logic