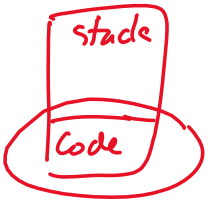
Jon 112 Dis 11

Tuesday, November 6, 2018 11:04 AM

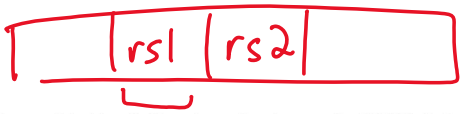
CS 61C Fall 2018

Single-Cycle Datapath

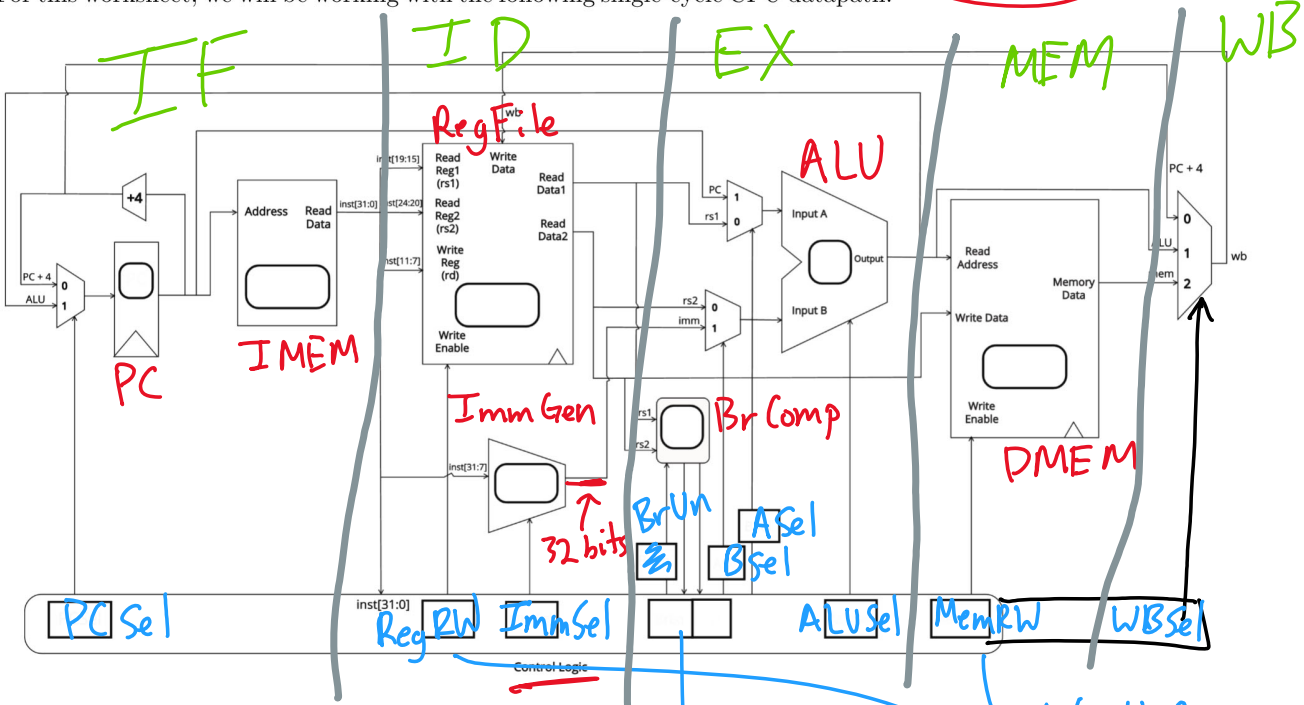
Discussion 11: November 5, 2018



1 Single-Cycle CPU



1.1 For this worksheet, we will be working with the following single-cycle CPU datapath:



(a) On the datapath above, fill in each **round** box with the name of the datapath component, and each **square** box with the name of the control signal.

(b) Explain what happens in each datapath stage.

IF Instruction Fetch

- get inst from mem

ID Instruction Decode

- figure out what to do w/ inst

EX Execute

- computations

MEM Memory

- store / read data from mem

WB Writeback

- write result to reg

1.2 Fill out the following table with the control signals for each instruction based on the datapath on the previous page. Wherever possible, use * to indicate that what this signal is does not matter.

	BrEq	BrLT	PCSel	ImmSel	BrUn	ASel	BSel	ALUSel	MemRW	RegWEn	WBSel
add ori	*	*	0	*	*	0	0	add	0	1	1
lw											
sw	*	*	0	S	*	0	1	add	1	0	*
beq											
jal bltu	*	*	1	UJ	*	1	1	add	0	1	0

1.3 **Clocking Methodology**

- A **state element** is an element connected to the clock (denoted by a triangle at the bottom). The **input signal** to each state element must stabilize before each **rising edge**.
- The **critical path** is the longest delay path between state elements in the circuit. If we place registers in the critical path, we can shorten the period by **reducing the amount of logic between registers**.

For this exercise, assume the delay for each stage in the datapath is as follows:

IF: 200 ps ID: 100 ps EX: 200 ps MEM: 200 ps WB: 100 ps

(a) Mark the stages of the datapath that the following instructions use and calculate the total time needed to execute the instruction.

	IF	ID	EX	MEM	WB	Total Time
add ori	X	X	X		X	600
lw	X	X	X	X	X	800 ps
sw	X	X	X	X		700
beq						
jal bltu	X	X	X		X	600

slowest

(b) Which instruction(s) exercise the critical path? lw

(c) What is the fastest you could clock this single cycle datapath? 1/800 ps = 1.25 GHz

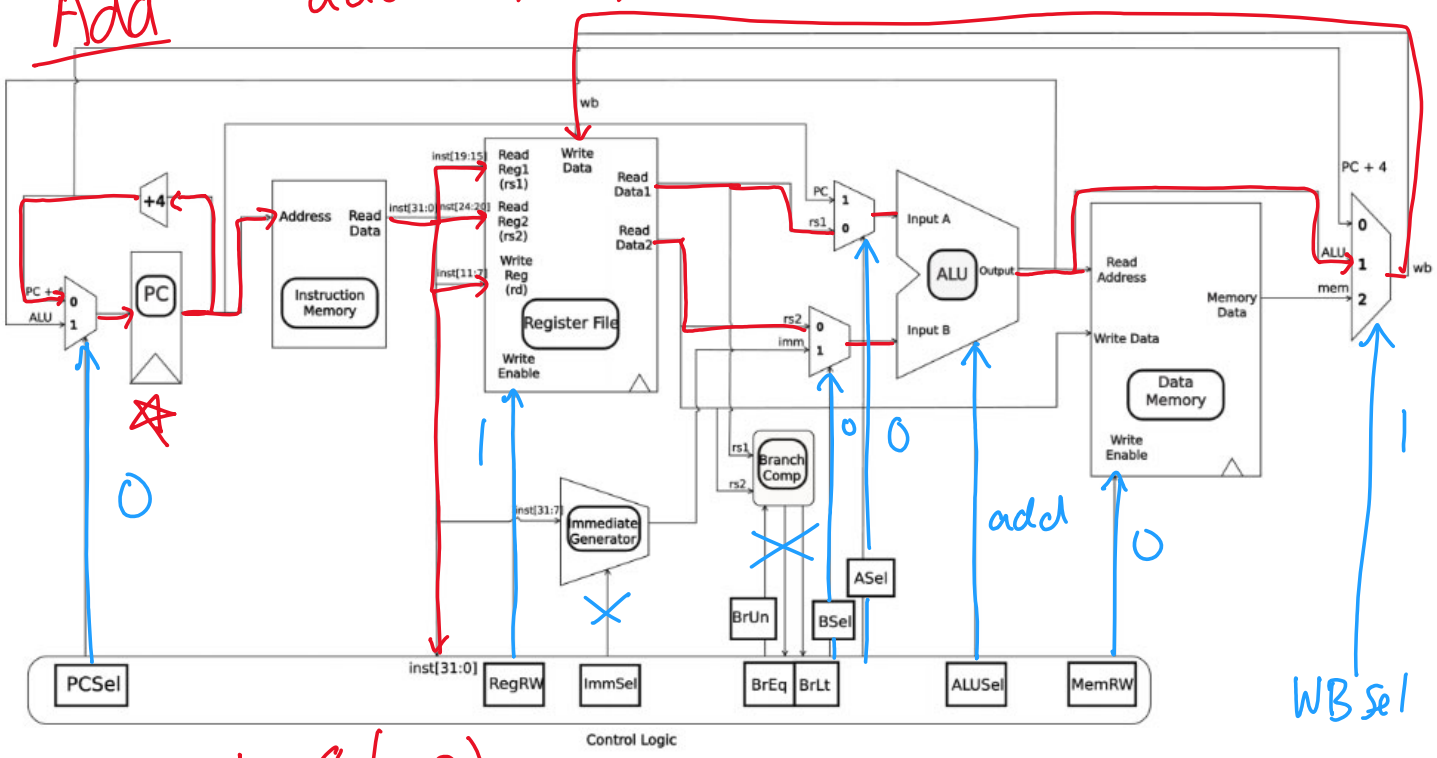
(d) Why is the single cycle datapath inefficient? idle components

(e) How can you improve its performance? What is the purpose of pipelining?

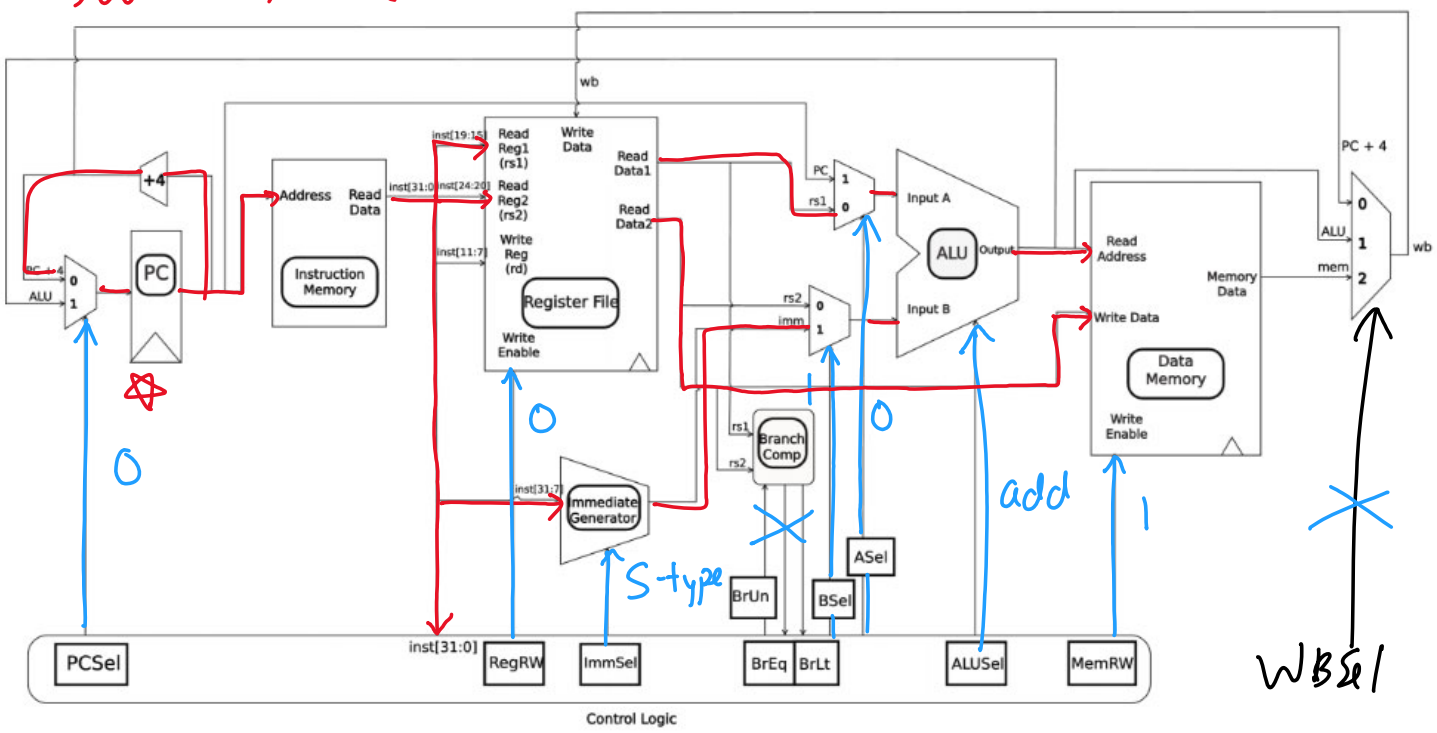
mult inst. at same time

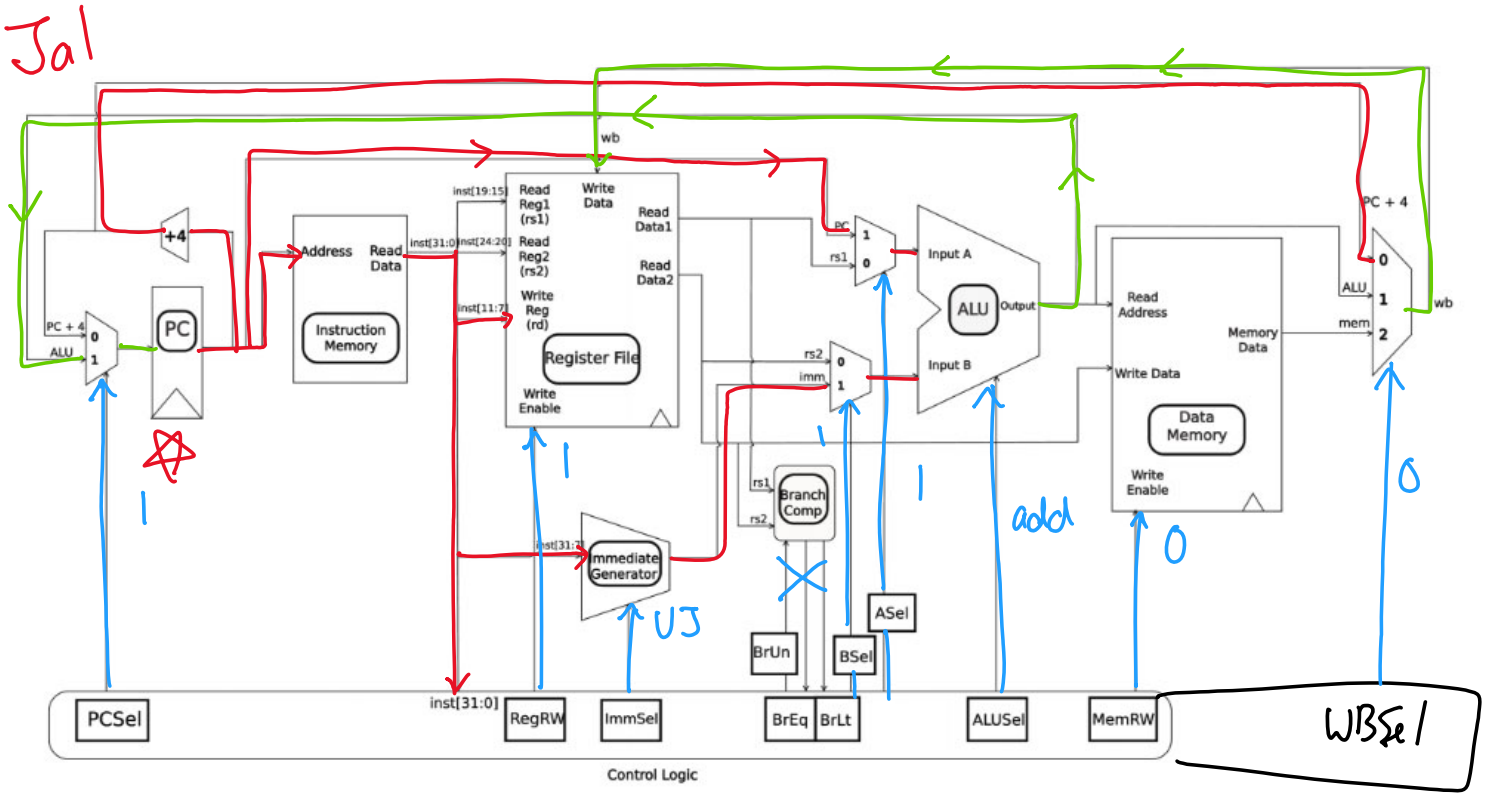
Add

add rd, rs1, rs2



sw x1, 8(x2)




Jal
wb
+4
PC + 4
ALU
PC
Address
Read Data
Instruction Memory
inst[31:0]
inst[19:15]
inst[24:20]
inst[11:7]
Read Reg1 (rs1)
Read Reg2 (rs2)
Write Reg (rd)
Write Data
Read Data1
Read Data2
Register File
Write Enable
PC
rs1
rs2
imm
Input A
Input B
ALU
Output
Read Address
Memory Data
Write Data
Data Memory
Write Enable
mem
Immediate Generator
Branch Comp
BrUn
BSel
ASel
BrEq
BrLt
ALUSel
MemRW
RegRW
ImmSel
PCSel
Control Logic
1
1
1
UJ
add
0
0
WBSel