Jon Discussion 9

Wednesday, July 18, 2018 12:22 AM

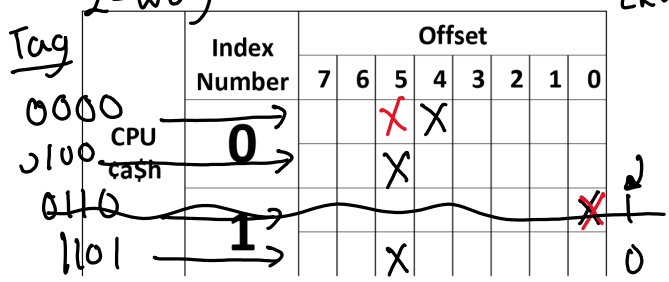
CS61C Discussion 9

N-Way Set Associative

Here's some practice involving a 2-way set associative cache, similar to last discussion's problem, except we have an 8-bit address space, classify each of the following accesses as a cache hit (H), cache miss (M), or cache miss with replacement (R). For any misses, list out which type of miss it is.

What is the T:I:O for this cache? T: 8-3-1=4 I: 1 O: $\log_2(8)=3$

2-Way



1. 0b0000 0100 M, comp
2. 0b0000 0101 H
3. 0b0110 1000 M, comp
4. 0b1100 1000 M, comp
5. 0b0110 1000 H
6. 0b1101 1101 M, comp + Replacement
7. 0b0100 0101 M, comp
8. 0b0000 0100 H
9. 0b1100 1000 M, capacity + Replacement

What is the hit rate of our 9 accesses?

Hits/total accesses

3/9 = 1/3

Analyzing C Code

```
#define NUM_INTS 8192
int A[NUM_INTS];  // A lives at 0x10000
int i, total = 0;
for (i = 0; i < NUM_INTS; i += 128) {A[i] = i;} // Line 1
for (i = 0; i < NUM_INTS; i += 128) {total += A[i];} // Line 2
```

Let's say you have a byte-addressed computer with a total memory of 1 MiB. It features a 16 KiB CPU cache with 1 KiB blocks.

1. How many bits make up a memory address on this computer? 2^{20}B $\log_2(2^{20})=20$
2. What is the T:I:O breakdown? Tag bits: 6 Index bits: 4 Offset bits: 10
3. Calculate the cache hit rate for the line marked Line 1: $128 \cdot 4 = 27 \cdot 2^2 = 2^9$ Block: 2^{10} 50%
4. Calculate the cache hit rate for the line marked Line 2: $8192 \cdot 4 = 2^{15}$ 2^{14} 50%

$\frac{16\text{KiB}}{1\text{KiB}} = 16 = 2^4$

backwards

Average Memory Access Time

AMAT is the average (expected) time it takes for memory access. It can be calculated using this formula:

AMAT = hit time + miss rate × miss penalty

Miss rates can be given in terms of either local miss rates or global miss rates. The *local miss rate* of a cache is the percentage of accesses into the particular cache that miss at the cache, while the *global miss rate* is the percentage of all accesses that miss at the cache.

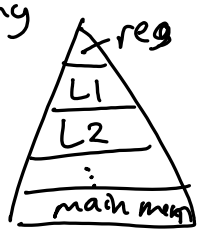
GMR: % of all accesses that miss here — cascading

LMR: % of accesses that miss

Exercises

Suppose your system consists of:

- A L1$ that hits in 2 cycles and has a local miss rate of 20%
- A L2$ that hits in 15 cycles and has a global miss rate of 5%
- Main memory hits in 100 cycles



1. What is the local miss rate of L2$?

$LMR = \frac{5\%}{20\%} = 25\%$

$25\% : 5\% = 20\% \cdot LMR$

$LMR = \frac{GMR}{\text{Access Rate}}$

2. What is the AMAT of the system?

$\cancel{\text{Inf}} \cdot GMR = \cancel{\text{Inf}} \cdot \text{AccessRate} \cdot LMR$

$AMAT = 2 + 20\% \cdot (15 + 25\% \cdot 100)$

$= 2 + \frac{1}{5}(15+25) = 2 + \frac{1}{5}(40) = 2 + 8 = 10$

3. Suppose we want to reduce the AMAT of the system to 8 or lower by adding in a L3$. If the L3$ has a local miss rate of 30%, what is the largest hit time that the L3$ can have?

Now, what if we have a cache system with the following properties. What is the AMAT?

- L1$ hits in 1 cycle (local miss rate 25%)
- L2$ hits in 10 cycles (local miss rate 40%)
- L3$ hits in 50 cycles (global miss rate 6%)
- Main memory hits in 100 cycles (always hits)

Flynn Taxonomy

1. Explain SISD and give an example if available.

Sngle Instr Sngle Data

2. Explain SIMD and give an example if available.

Sing Inst Mult Data

3. Explain MISD and give an example if available.

Mult Inst Sng Data

4. Explain MIMD and give an example if available.

MIMD Mult Inst Mult Data